AMENDMENTS TO THE CLAIMS

Claims 1-44. (canceled)

45. (previously presented) The integrated circuit of claim 68 wherein substantially all said additional dopants are displaced from said separated active regions by at least one hundred angstroms.

46. (previously presented) The integrated circuit of claim 68 wherein said separated active regions include elements of a memory device.

Claims 47-49. (canceled)

50. (previously presented) The integrated circuit of claim 68 wherein said additional dopants establish a field threshold voltage.

51. (previously presented) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions and wherein said additional dopants are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material.

52. (previously presented) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions and wherein said additional dopants are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material.

Claim 53. (canceled)

54. (previously presented) The memory device of claim 73 wherein the implanted ions establish a field threshold voltage.

Claim 55. (canceled)

56. (previously presented) The memory device of claim 73, wherein the first dielectric material has a thickness of at least about one hundred angstroms.

Claims 57-58. (canceled)

59. (previously presented) The memory device of claim 73 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 10 to 100 percent the depth of said first area filled with said first dielectric material.

60. (previously presented) The memory device of claim 73 wherein the ions are implanted into the substrate below said first area filled with said first dielectric material to a depth in a range of about 20 to 80 percent the depth of said first area filled with said first dielectric material.

Claims 61-67. (canceled)

68. (previously presented) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a plurality of active regions provided within said first region;

a field isolation region separating at least two of said active regions, wherein said field isolation region includes an isolation trench having a depth of about 3500 Angstroms, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a second area filled with a second dielectric material situated within said sidewalls, wherein said first dielectric material and said second dielectric material are different; and

a doped region within said first region below said second area, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher doping concentration are displaced away from said separated active regions.

69. (previously presented) The integrated circuit of claim 68 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

70. (previously presented) The integrated circuit of claim 68 wherein said additional dopants from said doped region are displaced away from said separated active regions by a distance at least equal to a sidewall thickness of said first area.

Claims 71-72. (canceled)

73. (currently amended) A memory device comprising:

a semiconductor substrate including a plurality of doped active regions, said semiconductor substrate having a first doping concentration;

a field isolation region separating at least two of said active regions, said field isolation region including an isolation trench, said isolation trench further including a first area filled with a first dielectric material forming at least sidewalls of said isolation trench, and a

second area filled with a second dielectric material situated within said sidewalls, said first dielectric material being different than said second dielectric material; and

an ion implanted region provided below and aligned with said second area, and having an increased doping concentration in an area of said substrate between said separated active regions, said increased doping concentration being higher than said first doping concentration of said substrate, wherein substantially all ions from said ion implanted region which increase said doping concentration are displaced away from said active regions and are aligned by ~~a distance at least equal to a sidewall thickness of said~~ the sidewalls of said isolation trench ~~first area filled with said first dielectric material, and wherein the sidewall thickness of said first area is less than about forty percent the width of the isolation region~~.

74. (previously presented) The memory device of claim 73 wherein said first area also includes said first dielectric material provided on a bottom of said isolation trench and said second dielectric material provided over said first dielectric material provided at said bottom.

Claims 75-76. (canceled)

77. (currently amended) An integrated circuit comprising:

a semiconductor substrate including a first region of a predefined conductivity type;

a field isolation region for separating said first region into at least two active regions, wherein said field isolation region includes an isolation trench, said isolation trench further including a first dielectric material forming sidewalls of said isolation trench and provided on a bottom of said isolation trench, and a second dielectric material situated within said sidewalls and provided over said first dielectric material, said first dielectric material being different than said second dielectric material;

at least a portion of a memory cell provided in at least one of said two active regions; and

a doped region formed within said first region and below said isolation trench, said doped region being of said predefined conductivity type and having a doping concentration higher than a doping concentration of said first region, wherein additional dopants in said doped region causing said higher dopant concentration are aligned by said sidewalls and are displaced away from said separated active regions.